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(54) **Trench etching using borosilicate glass mask**

(57) An improved method for forming semiconductor substrates using BSG avoids the problems associated with conventional TEOS hard mask techniques. The methods comprises providing a semiconductor substrate 1 and applying a conformal layer of borosilicate glass (BSG) 40 on the substrate. A photoresist layer 60 is then formed over the BSG layer and pattern to expose a desired portion of a layer underlying the photoresist layer. Anisotropical etching is then performed through the exposed portion of the underlying layer, through any other layers lying between the photoresist layer and the semiconductor substrate, and into the semiconductor substrate, thereby forming a trench in the semiconductor substrate. Preferably, one or more dielectric layers 10, 20 are present on the substrate surface prior to application of the BSG layer. One or more chemical barrier and/or organic antireflective coating layers 50 may be applied over the BSG layer between the BSG layer and the photoresist layer. The method is especially useful for forming deep trenches in silicon substrates with pad dielectric layers.

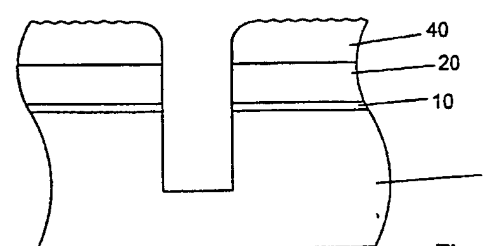

Figure 4

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Description

[0001] The present invention relates to the fabrication of trench structures in semiconductor substrates for use as capacitors and other devices.

[0002] The trench capacitor is a well known capacitor design for use in integrated circuits (IC), especially in IC memory devices. While variations exist in particular designs, trench capacitors are generally characterized by the formation of a deep trench in the semiconductor substrate (wafer) typically normal to the principal plane of the substrate. Deeper and narrower trenches are generally more desirable in that they reduce the area in the principal plane occupied by the capacitor. The reduction of the planar area occupied by the capacitor allows capacitors and other devices forming the integrated circuit to be placed more closely together on the chip. More dense packing of the integrated circuit design may enable improved circuit designs and improved circuit performance.

[0003] The formation of trench capacitors and other trench-based devices typically involves selectively etching the substrate whereby a trench is formed in the substrate. The composition of the substrate in the vicinity of the trench and the composition components arranged in the trench are manipulated to form the desired capacitor or other trench device. Thus, for example, the substrate area immediately underlying the trench may be doped with a charge carrier species, portions of the trench may be lined with a dielectric material, the trench may be back filled with a charge storage material, etc.

[0004] In many instances, it is desirable to form layers on the substrate surface prior to forming the desired trenches in the surface. For example, one or more "pad" dielectric (oxide and/or nitride) layers may be applied to the substrate surface prior to formation of the trench. These dielectric layers are typically needed outside the trench as part of the ultimate circuit structure or as part of the overall circuit fabrication process.

[0005] General methods for forming trenches are well known. Typically, a TEOS (tetraethyl orthosilicate) hard mask is deposited over the dielectric layers by chemical vapor deposition. A photoresist layer is applied over the TEOS layer and is patterned corresponding to the desired trench locations on the substrate. The substrate with the patterned photoresist is then etched so that trenches are formed in the substrate. The substrate is then subjected to further processing which may vary depending on the design of the integrated circuit, the desired performance level for the circuit, etc. Typically, the trenches will be used to form trench capacitors.

[0006] The trench formation method using a TEOS hard mask is widely used. See for example US patents 5,656,535; 5,348,905; 5,362,663; 5,618,751 and 5,657,092, the disclosures of which are incorporated herein by reference. Unfortunately, the current process is problematic since it is difficult to remove the TEOS layer after trench formation (e.g. prior to formation of the buried plate) without adversely affecting existing oxide structures such as pad oxides. Thus, the removal of the TEOS layer must be delayed to a further point in the fabrication process. In the course of the delay, the underlying layers such as the pad nitride layer may be adversely affected (e.g. they may lose uniformity, etc.).

[0007] Accordingly, the invention provides a method of forming a trench in a semiconductor substrate, said method comprising:

(a) providing a semiconductor material substrate;
(b) applying a conformal layer of borosilicate glass (BSG) on said substrate;
(c) forming a patterned photoresist layer over said BSG layer, whereby a portion of a layer underlying said photoresist layer is exposed;
(d) anisotropically etching through said exposed portion of said underlying layer, through any other layers lying below said photoresist layer, and into said semiconductor material, thereby forming a trench in said semiconductor material substrate.

[0008] In a preferred embodiment, said etching is performed by reactive ion etching and said BSG layer is formed by chemical vapor deposition. The BSG layer applied in step (b) preferably has a thickness of about 500-1000 nm (600-700 nm is particularly suitable) and has a boron content of at least about 5 wt.%. Preferably said semiconductor material is selected from the group consisting of silicon and doped silicon, and the trench is at least about 3 microns in depth (more especially 4-10 microns).

[0009] Generally step (d) comprises etching the BSG layer whereby the pattern from the photoresist layer is transferred to the BSG layer, stripping any remaining photoresist on the substrate, and etching said trench in the semiconductor substrate, and then said BSG layer is removed from said substrate after step (d), for example by contacting said BSG layer with an HF-containing vapor.

[0010] In the preferred embodiment there are one or more conformal dielectric layers (typically one containing a nitride) formed on said substrate prior to step (b) and said BSG layer is applied over said dielectric layer(s) in step (b). A particularly beneficial arrangement is for two dielectric layers to be formed on said substrate prior to step (b), said two dielectric layers consisting of a silicon oxide layer (typically with a thickness of about 0.5-1.5 nm) closest to said substrate and a nitride layer (typically with a thickness of about 150-300 nm) applied over said silicon oxide layer.

[0011] The preferred embodiment also has a chemical barrier layer (such as sputtered silicon) applied over said BSG layer prior to step (c) such that said chemical barrier layer lies between said BSG layer and said photoresist layer and prevents migration of boron from said BSG to said photoresist layer.

[0012] The preferred embodiment further has a con-

formal organic antireflective coating layer (comprising a poly (arylether) polymer for example) applied over said BSG layer (and the chemical barrier layer if present) prior to step (c) whereby said antireflective coating layer lies between said BSG layer and the patterned photoresist layer formed in step (c).

[0013] Such trench forming methods for semiconductor substrates avoid the problems associated with conventional TEOS hard mask techniques, and are particularly useful for forming deep trenches in silicon substrates with pad dielectric layers.

[0014] Thus a trench can be formed in a semiconductor substrate by (a) providing a semiconductor substrate; (b) applying a conformal layer of borosilicate glass (BSG) on the substrate; (c) forming a patterned photoresist layer over the BSG layer whereby a portion of a layer underlying the photoresist layer is exposed; and (d) anisotropically etching through the exposed portion of the underlying layer, through any other layers lying between the photoresist layer and the semiconductor substrate, and into the semiconductor substrate, thereby forming a trench in the semiconductor substrate. Thus the etching step comprises etching through said said BSG layer and any other intervening layers that may be present (eg antireflective coating layer, chemical barrier layer, or dielectric layer(s)).

[0015] In the preferred embodiment, one or more dielectric layers are present on the substrate surface prior to application of the BSG layer. One or more chemical barrier and/or organic antireflective coating layers may be applied over the BSG layer between the BSG layer and the photoresist layer. Step (d) may comprise discrete steps of etching the pattern in the BSG mask (mask open etch) followed by etching into the substrate (trench etch). The BSG layer is removed after trench formation.

[0016] An embodiment of the invention will now be described in detail by way of example only with reference to the following drawings:

Figure 1 is a schematic cross section of a silicon substrate with a BSG hard mask;
Figure 2 is a schematic cross section of the silicon substrate with a BSG hard mask of Figure 1 with applied chemical barrier and photoresist layers;
Figure 3 is a schematic cross section of the substrate with applied layers of Figure 2 after mask open etch;
Figure 4 is a schematic cross section of the substrate with applied layers of Figure 3 at the completion of trench etching; and
Figure 5 is a schematic cross section of the substrate with applied layers of Figure 4 on removal of the remaining BSG layer.

[0017] An example of one embodiment of the invention is schematically illustrated in Figures 1-5 (the relative dimensions shown in the figures are not to scale). It will also be appreciated that for simplicity, the figures illustrate the formation of a single trench, although most typically the method described herein would be used to form a plurality of trenches in a given substrate.

[0018] In Figure 1, an initial substrate **1** is shown having pad dielectric oxide **10** and pad dielectric nitride **20** thereon. Above the pad dielectric layers is the applied BSG layer **40**. In figure 2, layer **50** represents an applied chemical barrier or antireflective coating layer and layer **60** represents a patterned photoresist layer showing an exposed underlying layer at **30**. Figure 3 shows an intermediate step in the trench etching where etching of the BSG hard mask ("mask open etch") has been completed. Typically, at least a portion (if not all) of the photoresist layer **60** would have been removed at this point. Where the photoresist has not been completely removed, it is preferably stripped prior to etching of the trench ("trench etch"). The remaining photresist (and organic byproducts/organic antireflective coating, if any) may be stripped by wet or dry etching using techniques known in the art. The photoresist is typically incompatible with the chemistry of the trench etch. Figure 4 shows the completion of the trench etching step. Etching to this point typically will result in some erosion of the BSG layer **40**. Lastly, Figure 5 shows the structure remaining after removal of the BSG layer. Advantageously, the planarity of dielectric layer **20** is generally well preserved.

[0019] The semiconductor substrate may be any conventional semiconductor substrate, preferably in wafer form. The semiconductor substrate is preferably monocrystalline. Silicon is the preferred semiconductor material. It may be possible to use a doped semiconductor substrate as the starting substrate depending on the overall integrated circuit design and intended use.

[0020] Although the formation of dielectric pad layers is not a necessary part of the invention, typically such pad layers are often employed in manufacturing processes where trenches are formed in the substrate. If pad dielectric layers are desired, they may be formed by any conventional technique. Preferably, the pad dielectric layers are formed by chemical vapor deposition. Preferably, the substrate is provided with at least two dielectric pad layers, the dielectric layer closest to the substrate preferably being an oxide (e.g. a silicon oxide). At least one of the dielectric layers is preferably a nitride such as silicon nitride, silicon oxynitride, etc. The pad dielectric layers are preferably conformal and substantially planar as applied to the substrate. If an oxide dielectric layer is used, it preferably has a thickness of about 5-15 nm, more preferably about 10 nm. If a nitride dielectric layer is used, it preferably has a thickness of about 150-300 nm, more preferably about 200-250 nm.

[0021] The BSG layer may be formed by any conventional technique. Preferably, the BSG layer is formed by chemical vapor deposition (e.g. atmospheric CVD or LPCVD) using techniques known in the art such as

those described in US Patents 3,751,314, 5,584,941, and 5,677,225, the disclosures of which are incorporated herein by reference. The BSG layer applied has a thickness of about 500-1000 nm, more preferably about 600-700 nm. The BSG layer has a boron content of at least about 5 wt.% measured as B_2O_3, more preferably about 5.5 - 5.6 wt.%. In general, excessive levels of boron are preferably avoided. That is, the boron content is preferably not more than what is needed to provide selective removal (relative to oxide, nitride and silicon) of the BSG layer after formation of the trench.

[0022] The use of chemical barrier or antireflective coating layers is not required, although in many instances, it is indeed preferable to use one or more chemical barrier and/or antireflective coating layers.

[0023] The function of the chemical barrier layer is to prevent unwanted interaction between boron in the BSG layer and the subsequently deposited photoresist layer. The need for a chemical barrier layer may depend on the photoresist composition used, the boron content of the BSG, etc. If used, a preferred chemical barrier layer is amorphous α-silicon. Such amorphous silicon may be formed by sputtering or chemical vapor deposition using techniques well known in the art. Preferably, sputtering is used. The amorphous silicon is preferably applied at a thickness of about 5-20 nm, more preferably about 10 nm.

[0024] Organic antireflective coating layers may be used alone or in combination with a separate chemical barrier layer. In some instances, the antireflective coating may provide sufficient chemical barrier effect such that the need for a separate chemical barrier (e.g., amorphous α-silicon) is avoided. If used, the antireflective coating is preferably applied immediately below the photoresist layer. If both a chemical barrier layer and an antireflective coating layer are used, the antireflective coating layer is preferably situated between the chemical barrier layer and the photoresist layer. Preferred antireflective coating materials comprise poly (arylether) polymer. The antireflective coating is preferably applied using conventional spin coating techniques.

[0025] The formation of the patterned photoresist layer may be done by any conventional technique. Typically, a photoresist layer will be applied to the uppermost layer on the substrate. The photoresist layer is then patternwise exposed to a suitable radiation wavelength to induce a change in one or more characteristics (typically relative solubility) for the exposed regions of the resist layer. The patternwise exposed photoresist is then developed (e.g. by treatment with a solvent) to reveal the desired pattern of exposed locations (e.g. 30 in Figure 2) in the layer underlying the photoresist which correspond to the desired trench locations.

[0026] The substrate with the patterned photoresist layer is then anisotropically etched to selectively remove the portions of the layers directly under the exposed locations in the photoresist pattern including a portion of the semiconductor substrate thereby forming the desired trenches. The etching may be performed by any conventional anisotropic etching technique such as reactive ion etching or some other dry etching technique. Preferably, the etching involves the use of one or more halogen compounds. The etching step may involve the use of different combinations of etching conditions and techniques as the etching progresses through the various layers. Preferably, the etching comprises (1) a mask open etch where the pattern from the photoresist layer is transferred to the BSG mask (as shown in Figure 3), (2) stripping of any remaining photoresist on the substrate, and (3) trench etch in the semiconductor substrate. Typically, a portion of the BSG layer itself may be removed in the course of the trench etch step. This is preferably conducted until the trench formed has a depth in the semiconductor substrate of at least about 3 microns, more preferably about 4-10 microns. In some instances, post-etch cleaning steps may be employed to removed residues present in the trench.

[0027] Once the etching is completed, the remaining BSG layer may be removed. The BSG layer is preferably removed prior to further processing of the substrate. The BSG layer is preferably selectively removed by contacting the BSG layer with an HF-containing vapor. Alternatively, liquid etching techniques using a combination of HF and sulfuric acid may be used. Examples of suitable HF treatments are disclosed in US patent 5,658,417, the disclosure of which is incorporated herein by reference. Advantageously, the BSG layer can be removed in a highly selective manner relative to the silicon substrate and the pad dielectric layers. Typically, the BSG removal step will leave a substantially planar dielectric (nitride) surface.

[0028] The substrate with the formed trenches may then be subjected to known manufacturing techniques to produce the trench-based components and other devices making up the desired integrated circuit design.

[0029] Thus an improved method of forming trenches in semiconductor substrates has been described which avoids the disadvantages of TEOS hard mask processes, and which is especially useful where the substrate has pad dielectric layers applied prior to trench formation such as is typically done in the formation of trench capacitors.

Claims

1. A method of forming a trench in a semiconductor substrate, said method comprising:

   (a) providing a semiconductor material substrate (1);
   (b) applying a conformal layer of borosilicate glass (BSG) (40) on said substrate;
   (c) forming a patterned photoresist layer over said BSG layer, whereby a portion of a layer

(30) underlying said photoresist layer is exposed;

(d) anisotropically etching through said exposed portion of said underlying layer, through any other layers lying below said photoresist layer, and into said semiconductor material, thereby forming a trench in said semiconductor material substrate.

2. The method of claim 1 wherein said etching is performed by reactive ion etching.

3. The method of any preceding claim wherein said BSG layer is formed by chemical vapor deposition.

4. The method of any preceding claim wherein the BSG layer applied in step (b) has a thickness of about 500-1000 nm.

5. The method of claim 4 wherein the BSG layer applied in step (b) has a thickness of about 600-700 nm.

6. The method of any preceding claim wherein said semiconductor material is selected from the group consisting of silicon and doped silicon.

7. The method of any preceding claim wherein said BSG layer is removed from said substrate after step (d).

8. The method of claim 7 wherein said removal comprises contacting said BSG layer with an HF-containing vapor.

9. The method of any preceding claim wherein said trench formed in step (d) has a depth in said substrate of at least about 3 microns.

10. The method of claim 9 wherein said depth is about 4-10 microns.

11. The method of any preceding claim wherein said BSG layer has a boron content of at least about 5 wt.%.

12. The method of any preceding claim wherein step (d) comprises etching the BSG layer whereby the pattern from the photoresist layer is transferred to the BSG layer, stripping any remaining photoresist on the substrate, and etching said trench in the semiconductor substrate.

13. The method of any preceding claim wherein one or more conformal dielectric layers (10, 20) are formed on said substrate prior to step (b) and said BSG layer is applied over said dielectric layer(s) in step (b).

14. The method of claim 13 wherein at least one of said dielectric layers (20) contains a nitride.

15. The method of claim 14 wherein two dielectric layers are formed on said substrate prior to step (b), said two dielectric layers consisting of a silicon oxide layer (10) closest to said substrate and a nitride layer (20) applied over said silicon oxide layer.

16. The method of claim 15 wherein said silicon oxide dielectric layer has a thickness of about 0.5-1.5 nm.

17. The method of claim 15 or 16 wherein said nitride layer has a thickness of about 150-300 nm.

18. The method of any preceding claim wherein a chemical barrier layer (50) is applied over said BSG layer prior to step (c) such that said chemical barrier layer lies between said BSG layer and said photoresist layer and prevents migration of boron from said BSG to said photoresist layer.

19. The method of claim 18 wherein said chemical barrier layer is sputtered silicon.

20. The method of any preceding claim wherein a conformal organic antireflective coating layer (50) is applied over said BSG layer prior to step (c) whereby said antireflective coating layer lies between said BSG layer and the patterned photoresist layer formed in step (c).

21. The method of any preceding claim wherein said antireflective coating comprises a poly (arylether) polymer.

22. The method of any preceding claim, wherein said etching step comprises etching through said antireflective coating layer (if present), said chemical barrier layer (if present), said BSG layer and said dielectric layer(s) (if any).

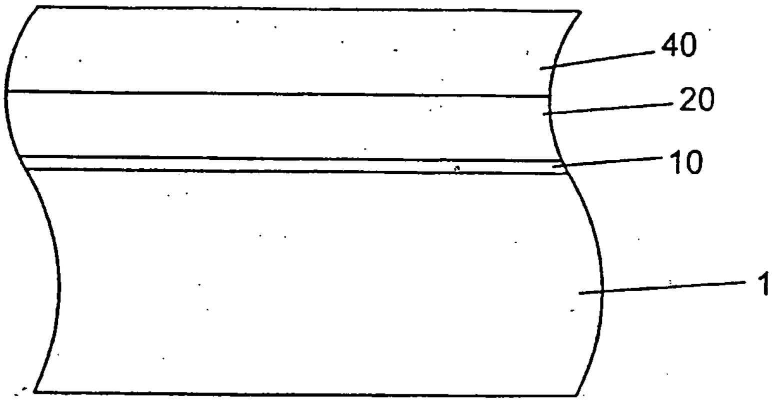

Figure 1

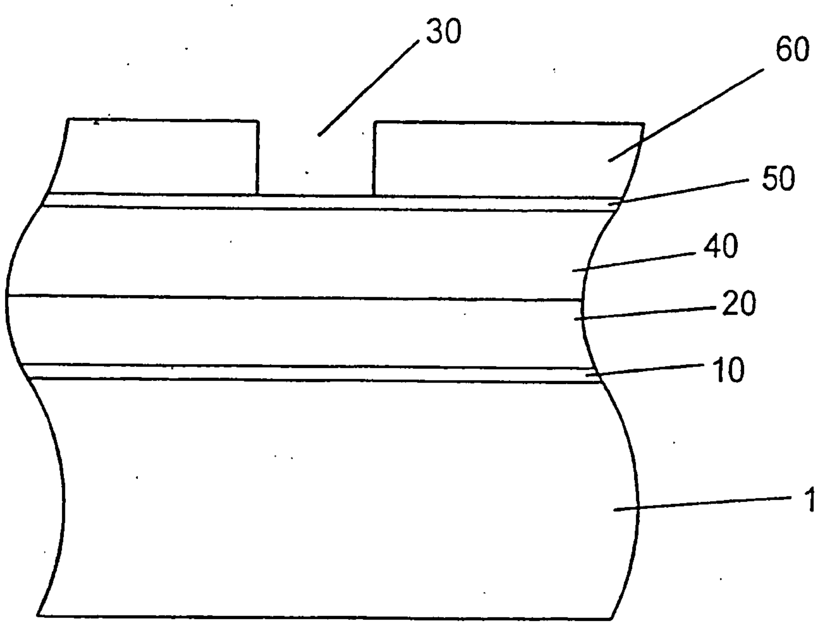

Figure 2

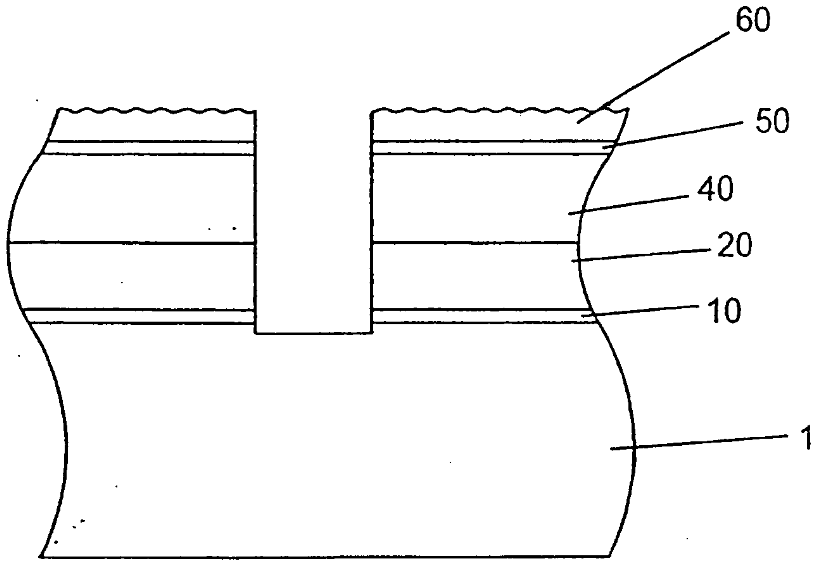

Figure 3

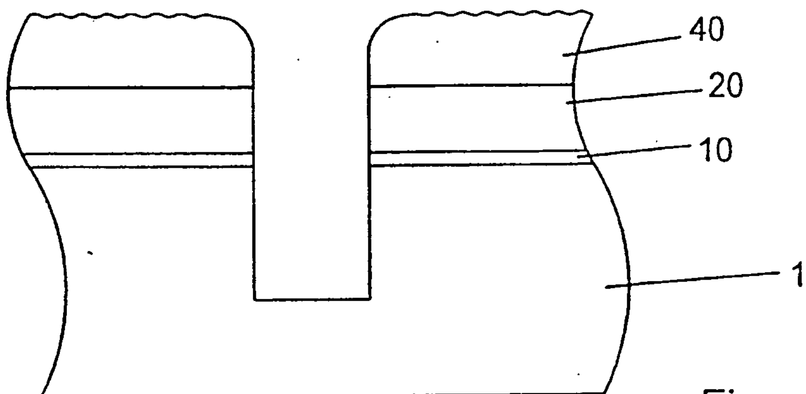

Figure 4

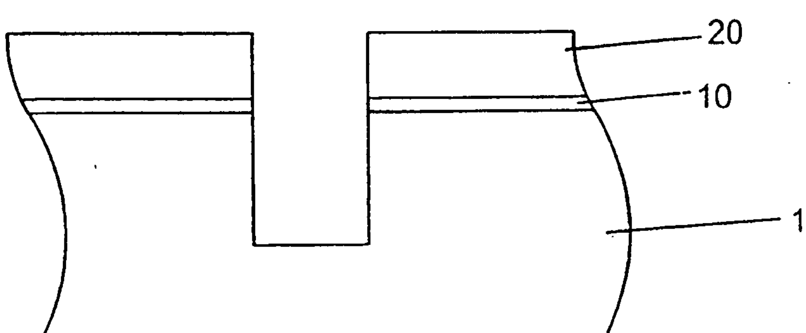

Figure 5